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Precision Engineering 30 (2006) 387–395
PRECISION ENGINEERING
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Design and prototyping of Stark atom chip for electric trapping of laser-cooled atoms

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Received 13 June 2005; received in revised form 27 October 2005; accepted 15 November 2005
Available online 13 February 2006

Abstract

An electric trapping of laser-cooled neutral strontium (Sr) atoms on a chip with micro-electrodes has been successful. The device is called "Stark atom chip" since it makes use of Stark effects on neutral atoms in electric fields. In this paper, our design and prototyping of the Stark atom chip with high aspect ratio electrodes precisely built on a surface are described. The functional requirements of the chip are specified during the discussion of designing the device. The authors design a novel process for fabrication of high aspect ratio electrodes. A focused ion beam (FIB) is used for precision fabrication of the prototype.

Keywords: Design; Prototyping; Stark atom chip; Electric trapping; Laser-cooled atoms; Functional requirement; Focused ion beam

1. Introduction

1.1. Purpose

The industry expects laser-cooled gas atoms [1] to serve as devices in quantum information processing (QIP) [2,3]. Extremely cold atoms will realize QIP when laser-cooled atoms are properly handled. Manipulating atoms on a chip may further open new possibilities of micro processing that shall also be classified as new QIP using atoms. Past works by others trapped and manipulated neutral atoms with spins by applying magnetic fields on magnetic atom chips [4,5]. Our past work discussed the Stark atom chip for electrically trapping of spinless neutral atoms [6–8].

This paper reports our work of designing a Stark atom chip by first identifying the functional requirements for performing atom trapping. We then produced a prototype and demonstrated the electric trapping of strontium (Sr) atoms.

1.2. Principle of electric trapping

This section first explains the mechanism of electric trapping of neutral atoms [9] with electrodes prepared on a surface [6].

An electric field $\boldsymbol{E}$ induces Stark shift in atoms. The Stark potential, U, is expressed $U = -(1/2)\alpha|\boldsymbol{E}|^2$, where α is the dipole polarizability of an atom. Fig. 1 shows the basic electrode structure for electric trapping. The structure has two diagonal pairs of electrodes separated by constant gaps that squarely run among the four columns on a glass substrate. When voltages $\pm V$ are applied to the two electrodes along the y-axis (Fig. 1), the Stark shift forms a saddle potential with a trough in the y-direction (Fig. 2). Similarly, when the voltages $\pm V$ are applied on the x-axis pair, the saddle flips the high and low points with a trough along the x-axis. Switching these two potential configurations at a constant frequency dynamically stabilities atoms near the center of the four electrodes. Note that

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doi:10.1016/j.precisioneng.2005.11.006

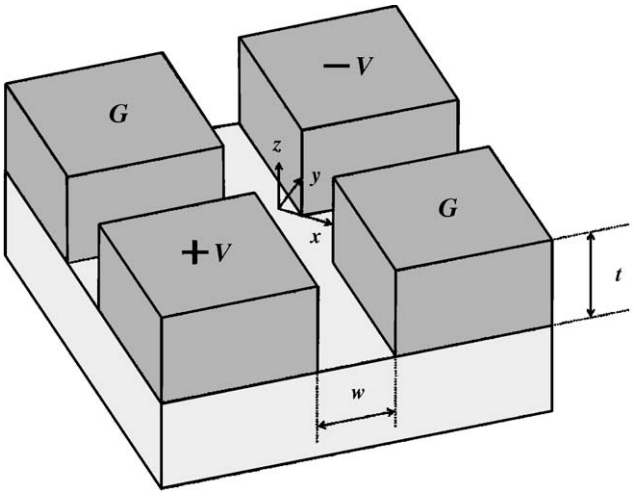

Fig. 1. Configuration of electrodes.

in either potential configuration, a static confining potential for atoms along z-axis are formed. Therefore, the scheme allows three-dimensional trapping of atoms.

1.3. Experimental procedure of electric trapping [7]

This section explains our procedure of demonstrating electric trapping of atoms. The chip is set so that its columns are pointing downwards (flipped upside down from the orientation in Fig. 1). The trapping experiment takes four steps. First, three-axis lasers work with the two reflections off the chip surface to cool and trap atoms near the chip (Fig. 3(a)). This technique is called magneto-optical trap (MOT [10,11]). Second, a pair of counter-propagating lasers transfers the atoms to the center of the electrode gaps [12] (Fig. 3(b)). Third, electric trapping takes place (Fig. 3(c)), and finally, the electrically trapped atoms are transferred out from the electrodes for observation (Fig. 3(d)). These processes are carried out in a chamber which is pumped down to ultrahigh vacuum ($\sim 10^{-10}$ Torr).

2. Design of Stark atom chip

2.1. Decision of electrode size

A numerical simulation allows us to find conditions for electric trapping [6]. Deeper Stark potential, i.e. a stronger electric field intensity ($\propto V/w$, Fig. 1) enables a deeper trap. Aiming for quantum computing on a chip, smaller electrode size ($\approx w$) and voltage V of a few volts or less have advantages for integration. The strontium atoms are laser-cooled at 1.5 mm below the chip (Fig. 3(a)), and then loaded to the electrodes (Fig. 3(b)) using a moving optical lattice with its beam diameter of 32 μm ($\lambda = 810$ nm, described later). We thus had to fix the electrode gaps to 50 μm; the most significant restriction on our Stark atom chip design. Further, a thicker electrode makes stabilization condition less stringent [7]. For the study in this paper, we set the aspect ratio to 2 for a stable trapping, and therefore the thickness t was 100 μm. The specification of the high aspect ratio 2 and a high fabrication precision (explained later) has made electrode fabrication difficult, and electrodes with such a high aspect ratio on a surface have been brought to realization. With the gap of the electrodes $w = 50$ μm, thickness $t = 100$ μm, and voltages $V = \pm 200$ V, typical switching frequency that satisfied the stability condition was 6 kHz. These parameters allow trapping Sr atoms with less than 15 μK in temperature (velocity ~ 4 cm/s) and $|r| < 8$ μm in size. A later Section 2.2.3 will explain the precision of the fabrication.

2.2. Functional requirements (FR) for Stark atom chip

We identified the following five functional requirements (FR) that the Stark atom chip must satisfy for electric trapping and its demonstration.

2.2.1. FR_1: high reflection (Ø 17 mm)

Three-axis lasers (L_1–L_6) cool and trap atoms (MOT). Two of these laser rays (L_2 and L_4 in Fig. 4) were reflections off the chip surface at 45° angles. The chip surface, thus, must provide

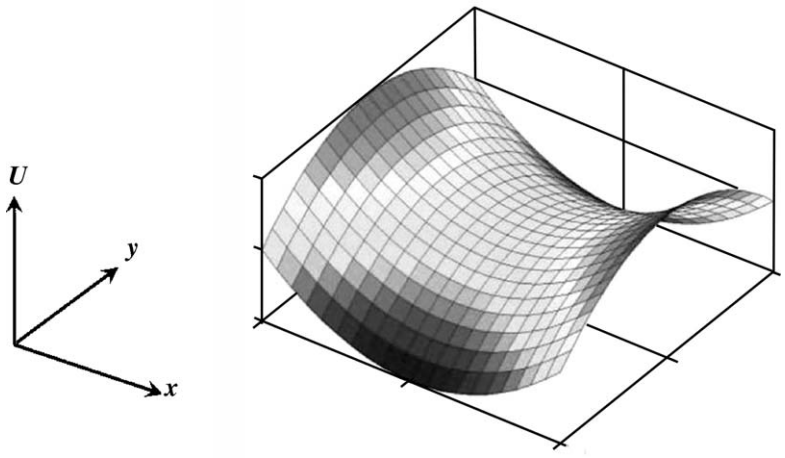

Fig. 2. Stark potential forms like a saddle shape ($z = 0$).

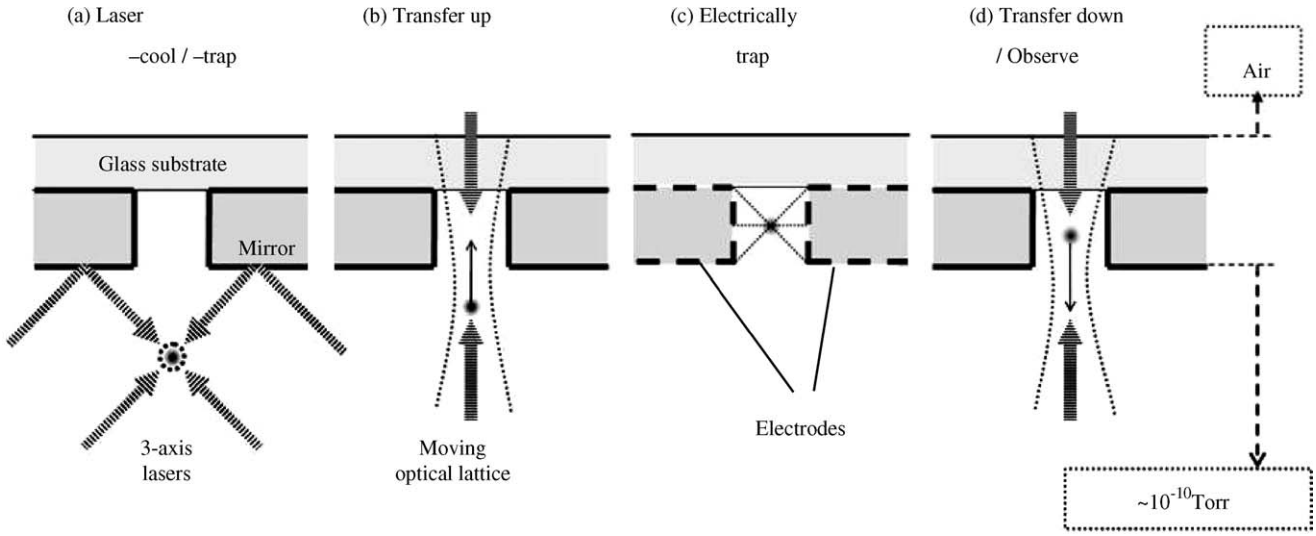

Fig. 3. Electric trapping and observing the trapping.

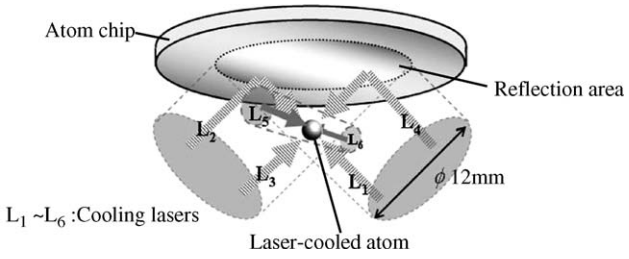

Fig. 4. Laser cooling and trapping with reflections from chip.

high reflectivity. The laser diameter for cooling and trapping was about 12 mm and the chip must reflect 95% or more of the original laser rays. We set our first functional requirement FR_1 to 95% or higher reflectivity in the area of 17 mm across. The laser wavelengths for the cooling and trapping were 460 and 689 nm.

2.2.2. *FR_2: optical transmission (Ø 50 μm)*

For transferring the trapped atoms up into the electric trapping area (Fig. 5), the center of the chip must be clear. The pair of lasers that face each other were 32 μm across and had to at least make 90% transmission for stable transferring. FR_2 was 90% optical transmission in an area of 32 μm across. The laser wavelength was 810 nm to assure stable transfer of strontium atoms.

2.2.3. *FR_3: high fabrication precision of electrodes*

Electric trapping requires high fabrication precision in the shape and surface of the electrodes. The trapping simulation predicted a precision requirement of ±1 μm to the 50 μm width gaps. The electrodes, with an aspect ratio of 2 (thickness/width = 100 μm /50 μm), has an acceptable slope of about

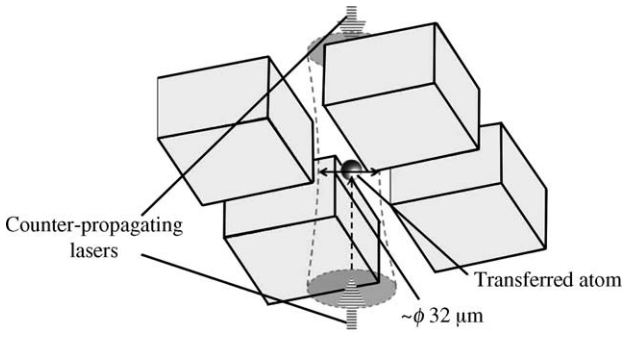

Fig. 5. Configuration of laser transferring.

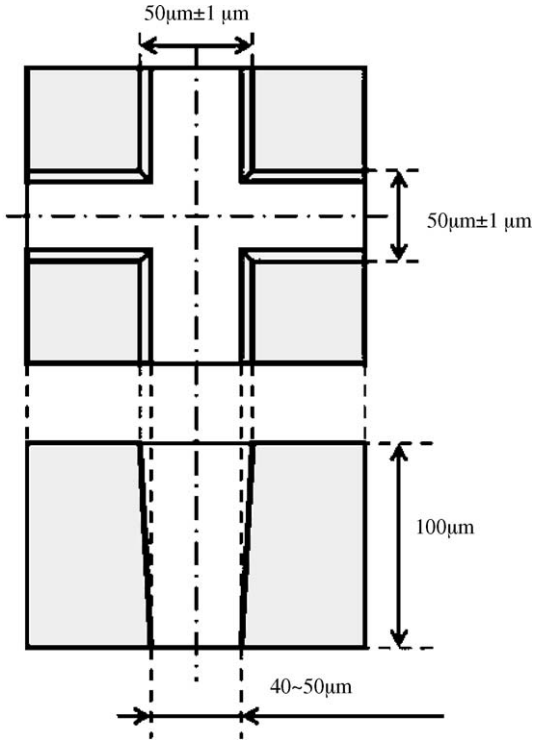

Fig. 6. Shape precision requirements of electrodes.

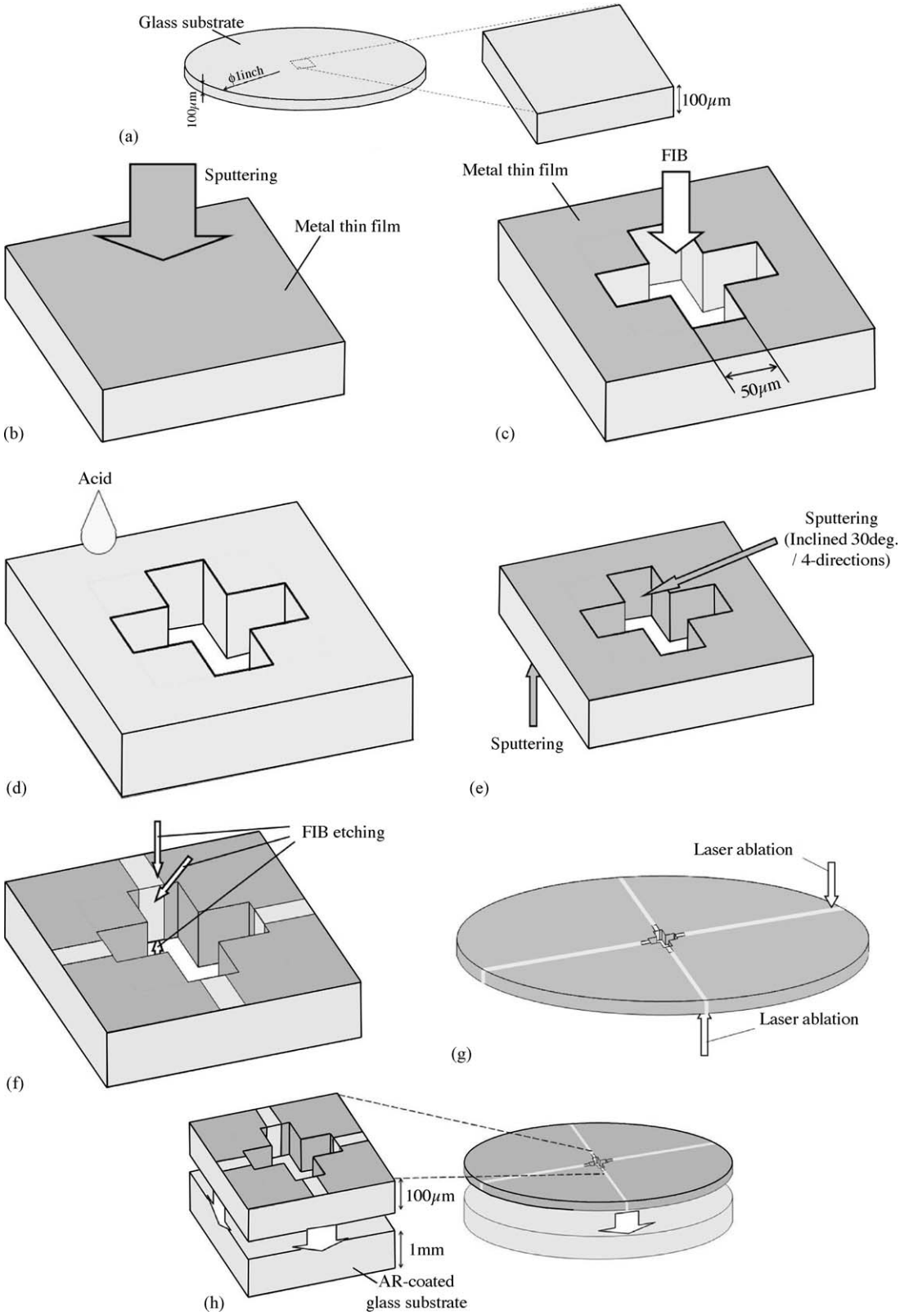

Fig. 7. Stark atom chip fabrication (a)–(f). (a) Prepare a glass substrate (Ø 1 in. × t 100 μm). (b) Sputter a metal thin film (MTF). (c) Etch a cross-shaped through hole. (d) Remove MTF with acid. (e) Deposit MTF on entire surface. (f) FIB etching. (g) Laser ablation. (h) Mount on AR (anti-reflection) coated glass substrate.

5/100. Their gap, therefore, may be as small as 40 μm, however, the symmetric precision must be within ±1 μm. Here, the symmetric precision of ±1 μm means that the tolerance of the distance from the symmetry plane to the electrode surface is within ±1 μm at any *xy*-plane. Simulations showed that if the electrodes have this symmetric precision, the trap size is almost the same as that of the ideal model (Fig. 6).

Further, the electrodes must have smooth surfaces that prevent electro-discharging. Our preliminary tests under vacuum showed that if the peak to valley of the electrode is kept to the nominal value within ±1 μm, the electro-discharge voltage is about ±400 V.

2.2.4. FR_4: thin electrode surfaces

In manipulating atoms with magnetic moments near metal surfaces, a proximity magnetic field caused by a thermal current due to Johnson noise voltage can heat up the atoms [13]. This heating can be reduced by employing thinner electrode surfaces, as it decreases the thermal current due to its higher resistance. Since the electric trapping does not require current flow as in the case of surface magnetic traps [4,5], the use of electrodes with high resistance does not alter the performance of the electric trapping. Rather the electric traps with such electrodes are well suited to manipulate atoms with spins [7]. This discussion gives the electrodes FR_4 of thin metal surfaces.

2.2.5. FR_5: sealing against vacuum and stiffness against pressure

Electric trapping takes place under ultrahigh vacuum ($\sim 10^{-10}$ Torr), and the Stark atom chip sits directly on the vacuum chamber port. The chip, therefore, must provide good sealing as well as stiffness against the uniform pressure. So FR_5 is sealing and stiffness against vacuum.

2.3. Design solution of Stark atom chip

Fig. 1 showed the basic structure of a Stark atom chip. Four rectangular columns covered with metal surfaces stand apart with gaps of 50 μm. MEMS (Micro Electro Mechanical Systems) processes, in this case, LIGA (Lithographie Galvanoformung und Abformung) process and dry etching (e.g. DRIE: deep reactive ion etching), are common in fabricating such 2.5D microstructures. LIGA, however, requires the post-processing of polishing. Furthermore, dry etching a 100 μm thick metal sheet deposited on a glass substrate, will leave a rough bottom surface. And the fourth functional requirement FR_4 (thin electrode surfaces) is hard to accomplish with these processes. We, therefore, propose a novel 3D structure forming process using thin film deposition and FIB (focused ion beam) etching. FIB successfully produces nano- or micro-structures without any masks. The process detects secondary electrons in a manner similar to SEM (scanning electron microscopy) to keep aligning the beam easy, and therefore, after-work fabrication is simple. The beam process has a large focal depth, and allows producing draft surfaces.

Fig. 7 shows the entire process of our Stark atom chip fabrication. Depositing a thin film of metal on an extremely flat glass substrate satisfies FR_1 (high reflection). We build the electrodes to form the chip base structure by penetrating a 100 μm thick glass substrate to satisfy FR_2 (optical transmission of trapping area). The beam diameter of the FIB we used was less than 1 μm. This fabrication process satisfies FR_3 (high precision of electrodes) and we will discuss more detail of this process later. Satisfying FR_5 requires a conventional approach of mounting the electrodes substrate onto another glass substrate with enough thickness to bear the air pressure, and applying epoxy adhesive with little out-gassing as a seal between the substrate and the vacuum chamber port.

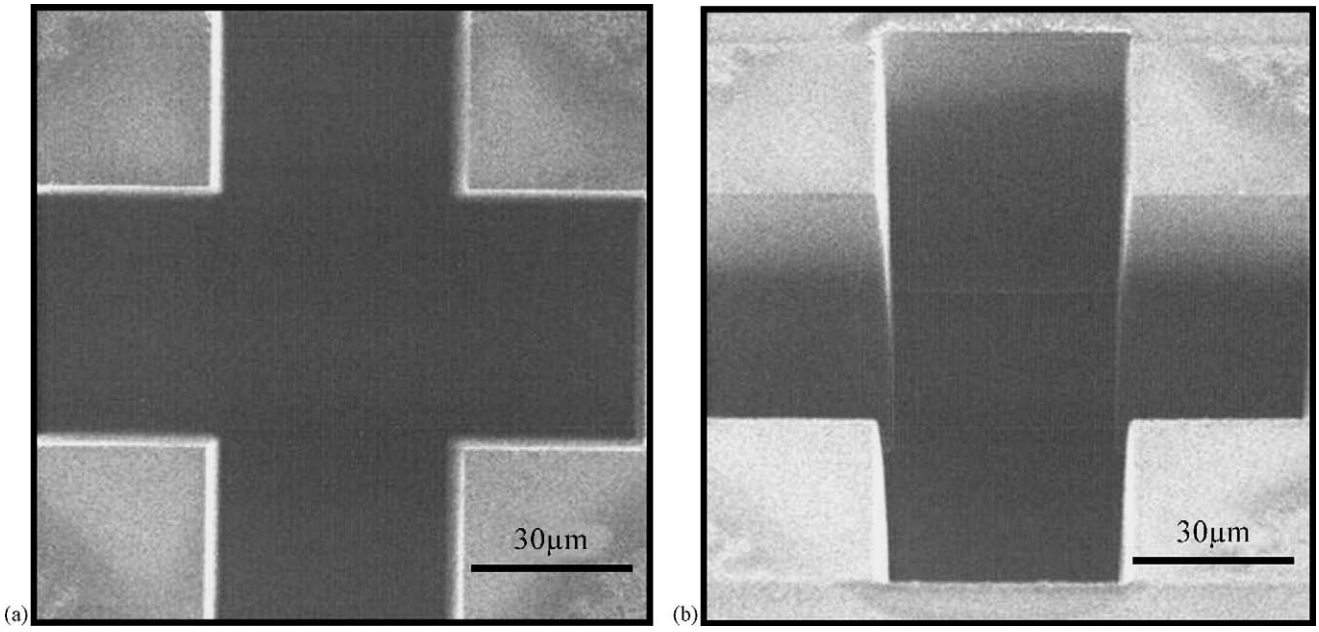

Fig. 8. FIB etching penetrated cross-shaped through holes (SIM images): (a) Top view; (b) Angled view (30°).

Table 1
Conditions of the FIB

Ion source	Liquid gallium ion
Beam current	24 nA
Beam acceleration voltage	30 kV
Beam diameter	900 nm
Dot interval	125 nm
Dwell time	32 μs
Scanning sequence	Fig. 9
Number of scans	12 cycles
Total fabrication time	72 h

3. Prototyping of Stark atom chip

3.1. Sub-processes of the prototyping

3.1.1. Sputtering a metal thin film for FIB etching (Fig. 7(b))

For FIB fabrication (Section 3.1.2), the glass substrate must be coated by conductive material. A 50 nm or thicker metallic surface would provide sufficient grounding. We thus sputtered a 50 nm thick nickel surface.

3.1.2. FIB etching the cross through hole (Fig. 7(c))

We applied FIB for fabricating the cross through hole on a 100 μm thick glass substrate. Fig. 8 shows the cross through hole we fabricated: the top view (a) shows that the top area has a precision within 1 μm, and the angled view (b), that the gap size at the bottom is 44 μm. This slope is acceptable and the symmetric precision is within 1 μm. The SIM (scanning ion microscope) images for verifying the precision have a resolution of 0.25 μm. Table 1 shows the conditions of the FIB etching process. Fig. 9 shows the sequence of scans we made for finishing the symmetric cross-shaped hole.

3.1.3. Removing the metal thin film with acid (Fig. 7(d))

The following processes removed the sputtered nickel thin film for FIB fabrication to control thickness of metal thin film. We used a 40% nitric acid solution. Further, we carried out ultrasonic cleaning in acetone and ethanol.

3.1.4. Ag thin film sputtering at angles (Fig. 7(e))

We sputtered thin films of silver (Ag) to produce thin electrodes. Thin films of silver provide high reflectivity in the visible range. For uniformly covering the electrodes with silver including the hole side walls, we defined five steps to this sputtering process. We tilted the chip by 30° to form the Ag thin film on one set of faces pointing at the same direction (Fig. 10). Repeating this tilted sputtering in the remaining three orthogonal directions completed covering the top and side surfaces. The fifth orientation completely flipped the chip over to cover its bottom face. The thickness of the side faces was 40 nm, and that of the top and back surfaces were 250 nm. Table 2 shows the sputtering conditions.

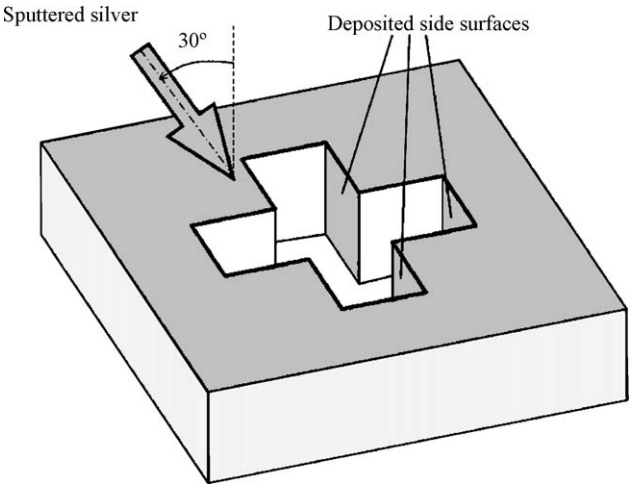

Fig. 10. Deposition of Ag thin film on side surfaces.

Table 2
Sputtering conditions of Ag thin film deposition

Method	Radio-frequency sputtering
RF power	80 kW
Sputtering gas	Argon plasma
Gas pressure	4×10^{-4} Torr
Deposition rate	120 nm/min (surface perpendicular to the sputtering direction)

3.1.5. FIB etching of metal thin film (Fig. 7(f))

This section explains the FIB metal etching of the metal thin film. Fig. 11(a) shows etching of the four side faces. We tilted the chip by 30° for etching these side faces, and etching one side face caused deposition of sputtered metal on the opposite face. Repeating the etching twice completely remove the deposited metal layer. Then grouping and extending the insulated side gaps, we etched the areas shown in Fig. 11(b). We etched an oversized area for each edge for its alignment with the laser ablation (Section 3.1.6). Tables 3a and 3b shows the FIB conditions for these processes. When all etching processes complete, all side surfaces have the same shape configuration.

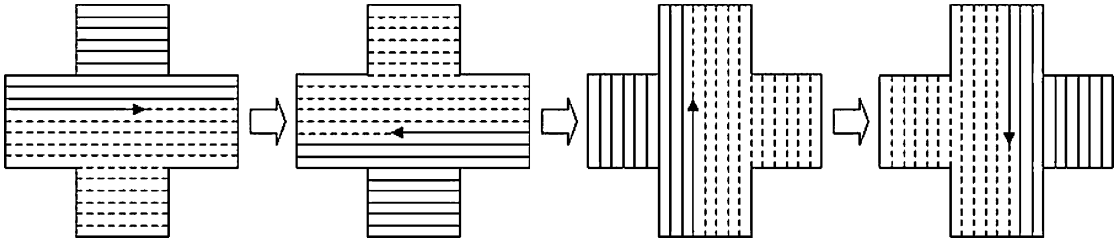

Fig. 9. Sequence of FIB scanning.

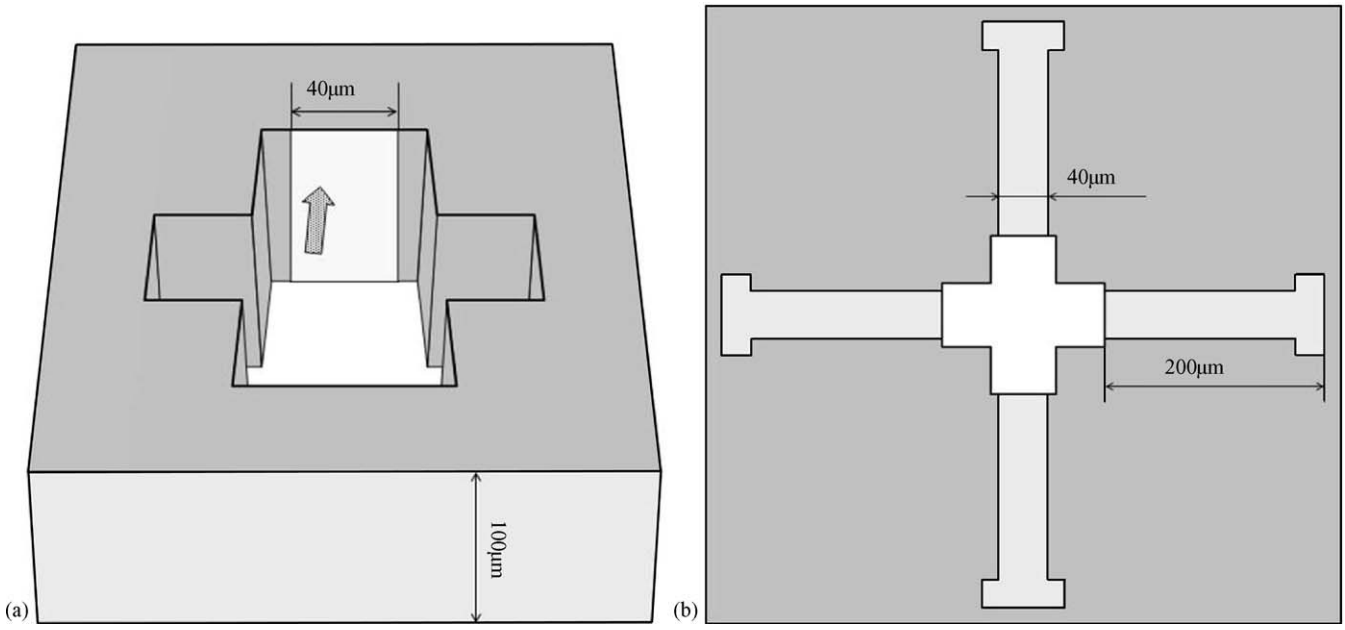

Fig. 11. Etching of metal thin film: (a) Inside surfaces; (b) Top and back surfaces.

Table 3a
FIB conditions for etching side faces (40 nm)

Beam current	0.9 nA
Beam diameter	150 nm
Dot interval	125 nm
Dwell time	128 μs
Scanning number	100 cycles × 4 (sides) × 3 (times)
Total fabrication time	110 min

Table 3b
FIB conditions for etching top and back surfaces (250 nm)

Beam current	20 nA
Beam diameter	900 nm
Dot interval	500 nm
Dwell time	128 μs
Scanning number	200 cycles × 4 (sides) × 2 (times)
Total fabrication time	160 min

3.1.6. Laser ablation in wide range (Fig. 7(g))

FIB fabrication is precision, however, its speed of material removal is relatively slow. For faster total machining time, we therefore, applied FHG YAG laser with conditions in Table 4, for isolating out the four electrodes by ablating the thin film out from the top and backsides of the chip.

Table 4
Laser specification and condition

Source	Continuous oscillation, fourth harmonic generation YAG (yttrium aluminum garnet), wavelength: 266 nm
Beam power	10 mW
Beam diameter	10 μm
Scanning speed	0.3 mm/s
Finalized gap	60 μm (10 scans pitched 5 μm)

3.2. Prototyped Stark atom chip

Fig. 12 shows a finished Stark atom chip. The image looks through the cross-shaped hole from the backside. The chip in this figure had cleaner thin film, produced in one set of scans, and we used this chip for our demonstration.

3.3. Equipment

The electrode chip was mounted on a 1 mm thick glass substrate made of BK7 and coated with anti-reflection (AR). The glass substrate was bonded to the chamber port with an epoxy material with little out-gassing ("Torr Seal" by VARIAN met this condition of little out-gassing under ultrahigh vacuum ($\sim 10^{-10}$ Torr)). This bonding material also provided a tight vacuum seal. The four electrodes were wired to the outside of the

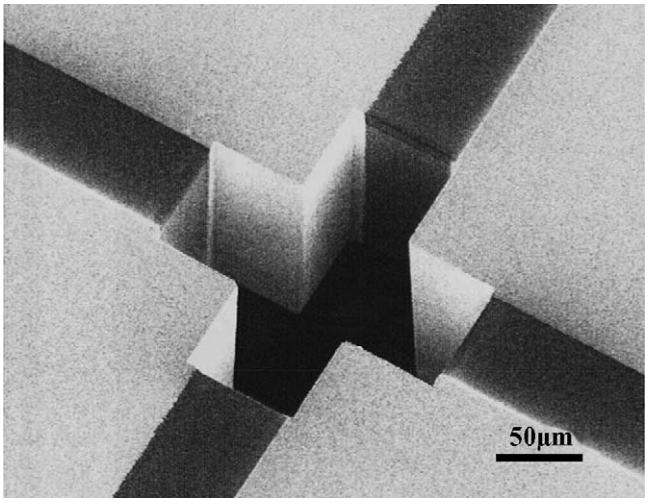

Fig. 12. SIM image of the Stark atom chip.

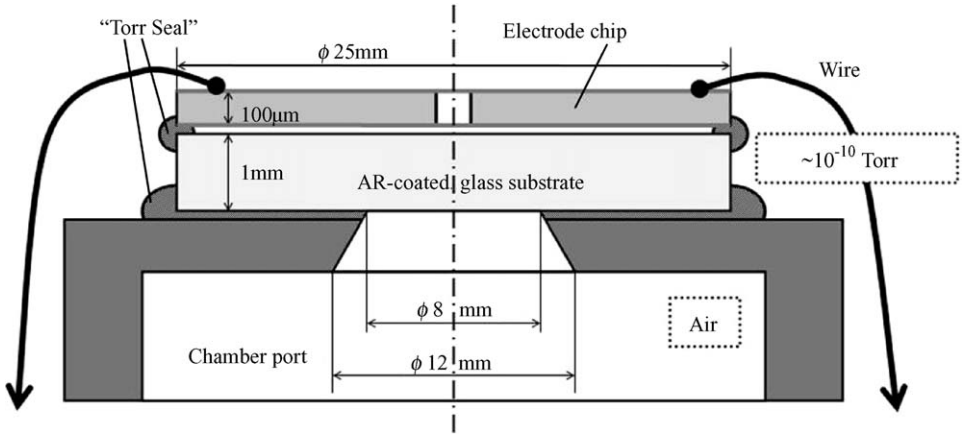

Fig. 13. Assembly around the vacuum chamber port.

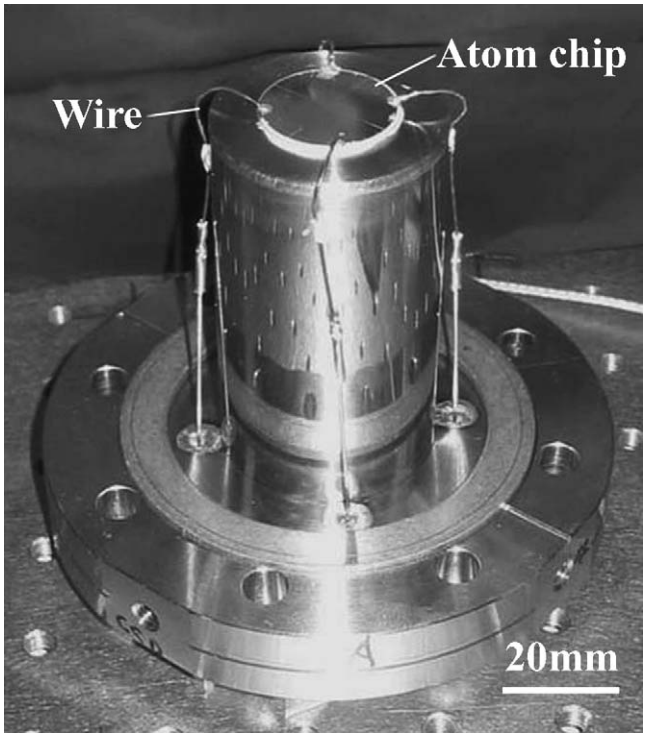

Fig. 14. Vacuum chamber mounted with substrates.

chamber. Fig. 13 shows the overall assembly around the chamber port in a cross-section. Fig. 14 shows the actual view of the Stark atom chip attached on the vacuum chamber.

4. Experimental result of electric trapping [7]

We show an experimental result of demonstrating electric trapping of ^{88}Sr atoms in the $^1S_0$ ground state. A CCD camera monitored atoms by the laser induced fluorescence on the $^1S_0$–$^1P_1$ transition. MOT lasers (Fig. 3(a)) cooled and trapped 10^5 of ^{88}Sr atoms with a temperature of 5 μK at the position of 1.5 mm below the electrodes. The atoms were then loaded into the optical lattice trap with a transfer efficiency of 50%. The trapped atoms were transferred up into the chip center by the moving optical lattice in 7 ms (Fig. 3(b)). After turning off the optical lattice, the electric trapping was performed for 5 ms (Fig. 3(c)). At this time, the temperature of the atoms was 7 μK. As described in Section 1.2, the Stark trap was operated with voltages of ±200 V and the switching frequency of 6 kHz. In order to observe the electrically trapped atoms, they were pulled out downwards by optical lattice (Fig. 3(d)). About 100 atoms were observed at this time. Using this observation scheme, we have studied the stability condition of the electric trap [7], which was well reproduced by numerical simulation [6].

5. Discussions

We described a design solution of a prototype Stark atom chip for demonstrating electric trapping on a surface. The next step is to extend this single Stark atom trap to an array of traps formed on a plane. By switching the electrodes in a controlled sequence shall allow us to transfer the atoms along the array. This process will lead to an atomic wave-guide similar to a "quantum CCD" [14].

Downscaling these electrodes to a few micro-meters would allow traps or transfer carried out by 5 V or less, which can be driven by TTL (transistor–transistor logic) [6]. The fabrication method we described in this paper could scale down to 1/10 of the size here, because FIB systems are available with beam sizes in tenths of what we used in our studies. FIB processes allow integrative fabrications from several 100 μm to about 1 μm, and the fabrication method we described in this paper is one of the universal solutions.

6. Conclusions

We identified the functional requirements for demonstrating electric trapping of laser-cooled atoms. We then designed and prototyped the Stark atom chip with high aspect ratio electrodes precisely built on a surface to perform the demonstration. The Stark atom chip trapped a measurable number of atoms as we intended.

Acknowledgements

The authors would like to thank J. Fujiki, S. Yamauchi, M. Tange for their help in carrying out the experiments and simulations, and also, T. Hamaguchi and K. Tsuchiya for their advices.

References

[1] Phillips WD. Laser cooling and trapping of neutral atoms. Rev Mod Phys 1998;70:721–41.
[2] Leibfried D, Blatt R, Monroe C, Wineland D. Quantum dynamics of single trapped ions. Rev Mod Phys 2003;75:281–324.
[3] Cirac JI, Zoller P. Quantum computations with cold trapped ions. Phys Rev Lett 1995;74:4091–4.
[4] Reichel J, Hänsel W, Hommelhoff P, Hänsch TW. Applications of integrated magnetic microtraps. Appl Phys B 2001;72:81–9.
[5] Bartenstein M, Cassettari D, Calarco T, Chenet A, Folman R, Brugger K, et al. Atoms wires: toward atom chip. IEEE J Quantum Electron 2000;36:1364–77.
[6] Katori H, Akatsuka T. Electric manipulation of spinless neutral atoms on a surface. Jpn J Appl Phys 2004;43:358–60.
[7] Katori H, Takamoto M, Kishimoto T, Hachisu H, Fujiki J, Higashi R, et al. Engineering stark potential for precision measurements: optical lattice clock and electrodynamic surface trap. In: Marcassa LG, Bagnato VS, Hermerson K, editors. Proceedings of the 19th international conference on atomic physics 2004 (ICAP2004), CP770, atomic physics 19. New York: American Institute of Physics; 2005. p. 112–22.
[8] Nagato K, Ohsige K, Ooi T, Tsuchiya K, Hamaguchi T, Nakao M. Fabrication of atom trap chip for quantum information processing. In: Proceedings of 19th ASPE annual meeting. 2004. p. 121–4.
[9] Shimizu F, Morinaga M. Electric trapping of neutral atoms. Jpn J Appl Phys Part 2 1992;31:L1721–3.
[10] Raab EL, Prentiss M, Cable A, Chu S, Pitchard DE. Trapping of neutral sodium atoms with radiation pressure. Phys Rev Lett 1987;59:2631–4.
[11] Metcalf HJ, Straten P. Laser cooling and trapping. Springer Verlag; 1999.
[12] Kuhr MS, Alt W, Schrader D, Müller M, Gomer V, Meschede D. Deterministic delivery of a single atom. Science 2001;293:278–80.
[13] Henkel C, Potting S. Coherent transport of matter waves. Appl Phys B 2001;72:73–80.
[14] Kielpinski D, Monroe C, Wineland DJ. Architecture for a large scale ion-trap quantum computer. Nature 2002;417:709–11.